JASON HO

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EDUCATION

University of Texas, Austin *Aug 2022 - Present*
Ph.D. Electrical and Computer Engineering in Computer Architecture **GPA: 3.96**
Thesis Topic: Design of Energy-Efficient Hybrid Analog/Digital Neuromorphic Architectures

University of Texas, Austin *Aug 2022 - Dec 2024*
M.S. Electrical and Computer Engineering in Computer Architecture **GPA: 3.96**
Relevant Coursework: Cross-Layer ML HW/SW Codesign, Parallel Computer Architecture, Prediction Mechanisms in Computer Architecture, ML for Computer Systems, Low Power Design

Brown University *Sept 2018 - May 2022*
Sc.B. Computer Engineering with Honors **GPA: 3.96**
Thesis: Tools for Understanding the Computational Behaviors of Biofilms
Relevant Coursework: VLSI Design, Digital Signal Processing, Operating Systems

RESEARCH EXPERIENCE

Graduate Researcher, SLAM Lab, UT Austin *Aug 2022 - Present*
Advisor: Professor Andreas Gerstlauer
• Researching the co-design of hybrid analog/digital neuromorphic (brain-like) computing systems that combine the efficiency of analog computing with the scalability of a digital backend
• Investigating the use of machine learning to create surrogate models of analog circuits, resulting in 3 orders of magnitude simulation speedup over SPICE with energy, latency and behavior estimation under 7%, 8%, and 2%, respectively
• Researching tradeoffs of novel devices such as RRAMs in hybrid neuromorphic architectures for spiking neural network acceleration

Undergraduate Researcher, SCALE Lab, Brown University *Jan 2021 - Jun 2022*
Advisor: Professor Sherief Reda and Professor Jacob Rosenstein
• Modeled bacterial biofilm coupling interactions as Kuramoto oscillators to investigate non-conventional oscillatory computing systems
• Developed super-resolution techniques for impedance tomography on a custom imaging and stimulation platform for oscillatory computing system exploration

PUBLICATIONS

J. Ho, E. Atayeter, T. Blottin, I. Joe, R. Sistrunk, B. Zhang, L. Solnica-Krezel, A. Gerstlauer, J. Wallingford, R. Gray, "Cilia.io: Computer vision and machine learning reveal spatial patterns of cilia beating dynamics in the spinal cord", in Cell Reports Methods, 2026. (in review)

J. Boyle, **J. Ho**, A. Aalund, Z. Houlton, A. Iman, I. Gonzalez, K. Jha, L. Lui, P. Shroff, R. Sam, S. Cardwell, F. Chance, A. Gerstlauer, "Bridging the Gap in Neuromorphic Co-Design with the SANA-FE Co-Simulation Framework", in IEEE Computer Special Issue: Convergence in Neuromorphic Sysgtems: From Circuit Innovation to Adaptive Cognition, 2026. (in review)

J. Ho, J. Boyle, L. Liu, A. Gerstlauer, "LASANA: Large-Scale Analog Surrogate Modeling for Neuromorphic Architecture Exploration", in International Symposium on Machine Learning for Computer-Aided Design (MLCAD), 2025.

J. Boyle, **J. Ho**, M. Plagge, S. Cardwell, F. Chance, A. Gerstlauer, "Exploring Dendrites in Large-Scale Neuromorphic Architectures," in International Conference for Neuromorphic Systems. (ICONS), 2025.

K. Hu, **J. Ho** and J. K. Rosenstein, "Super-Resolution Electrochemical Impedance Imaging with a 512×256 CMOS Sensor Array," in IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), 2022, doi: 10.1109/TBCAS.2022.3183856.

INVITED TALKS

"LASANA: Large-Scale Analog Surrogate Modeling for Neuromorphic Architecture Exploration", Qualcomm Internal Ph.D. Talk, July 2025.

POSTER PRESENTATIONS

"LASANA: Large-Scale Analog Surrogate Modeling for Neuromorphic Architecture Exploration", 6G @ UT Symposium, Austin, Texas, November 2025.

"LASANA: Large-Scale Analog Surrogate Modeling for Neuromorphic Architecture Exploration", iMAGiNE Consortium Student Poster Session, Austin, Texas, April 2025.

"LASANA: Large-Scale Analog Surrogate Modeling for Neuromorphic Architecture Exploration", AMD Poster Session, Austin, Texas, November 2024.

"LASGNA: Large-Scale Analog Surrogate Modeling for General Neuromorphic Architectures", MLCAD 2024, Snowbird Utah, September 2024.

ENGINEERING EXPERIENCE

GPU Power Architect Intern, Nvidia *May 2026 - Sept 2026*
• TODO

CPU Power Characterization and Modeling Intern, Qualcomm *Jun 2025 - Aug 2025*
• Characterized and modeled energy efficiency of the power management IC tree in future Oryon CPUs targeted for mobile and laptop applications

Power and Performance Lead/Architect Intern, AMD *May 2023 - Aug 2023*
• Characterized power and performance on future APU plus discrete GPU platforms focused on power allocation algorithms between the APU and GPU on GPU-bound benchmarks
• Owned and deployed an internal data analysis tool that linked Power BI and internal databases to automate multi-phasic statistical analysis of benchmark logs, providing a 100x speedup from previous methods
• Maintained, built, and ran benchmarks on 8 separate systems for power and performance characterization

VLSI Read Channel Design and Verification Intern, Seagate Technology *Jun 2022 - Aug 2022*
• Lead verification transition for the team from VMM to UVM environment while reusing as much code as possible
• Developed firmware initialization and configuration code for read channel UVM environment with functionality for large-scale read channel testbenches

VLSI Design and Verification Engineering Intern, Seagate Technology *May 2021 - Aug 2021*
• Designed and optimized RTL block to increase ECC correction throughput in the hard drive read pipeline
• Developed VMM infrastructure to verify the new RTL block robustly

FPGA Engineering Intern, Nabsys *Jun 2020 - Sept 2020*
• Developed parallel signal processing algorithms and state machines on Xilinx FPGAs for analysis of tagged DNA for whole genome sequencing

• Optimized FPGA design to reduce slices by 2x, while increasing throughput by 16x to process streaming of 128 nanopore sensors

Security Engineering Intern, Brown OIT *Apr 2019 - Sept 2019*
• Designed Copyright infringement scripts in Python that parsed DMCA emails, searched firewall logs, and verified infringement on University firewall traffic, saving non-technical staff over 3 hours of time per case or speedup of 30x
• Queried SQL databases to aggregate Crowdstrike data with firewall permit-deny traffic on real-time dashboards to display malicious traffic by optimizing firewall parsing by 20 times using regex

TEACHING AND MENTORING EXPERIENCE

ECE Graduate Peer Mentor, UT Austin *Aug 2023 - Present*
• Mentor group of 6-8 first-year Electrical and Computer Engineering graduate students through the transition to UT Austin

Master's Student Mentor, UT Austin *Aug 2023 - Jun 2025*
• Mentored master's student interested in pursuing a Ph.D. in computer architecture; Now pursuing a Ph.D. at Johns Hopkins University

EEMP Mentor, Science Mentorship Institute *Feb 2024 - Aug 2024*
• Mentor for two high school students interested in research, which culminated in a literature-review-based poster session

Head Teaching Assistant, ENGN 1640: Design of Computing Systems *Jan 2022 - May 2022*
• Ran office hours twice a week in the computing lab to help students build RISC-V processors on Altera FPGA boards
• Held conceptual hours for students and helped guide students toward designs optimized to minimize logic, or speed

Teaching Assistant, ENGN 1580: Communication Systems *Jan 2022 - May 2022*
Student TA Evaluation Score: 5.0 / 5.0
• Designed a final project for students to emulate communication across a physical channel amid noise and crosstalk on the channel.
• Held conceptual hours for students to further their understanding beyond the classroom

Head Teaching Assistant, CSCI 1600: Real-Time and Embedded Software *Sept 2021 - Dec 2021*
• Lead two lab sessions a week, teaching students Arduino and breadboarding on topics such as timers, interrupts, real-time operating systems, and sensors
• Held conceptual hours once a week for any students to come to as well
• Guided and provided advice to students for their final design projects

Mentor, MAPS (Matched Advising Program for Sophomores) *Jan 2021 - May 2022*
• Advised mentees interested in concentrating in Computer Engineering, Computer Science, or related fields on classes, research, and internship opportunities

Mentor, Brown School of Engineering *Jan 2021 - May 2022*
• Helped mentees devise plans on completing concentration requirements as well as providing advice on classes, research, internship opportunities, and approach to learning

Teaching Assistant, ENGN 0500: Digital Computing Systems *Jan 2021 - May 2021*
Student TA Evaluation Score: 4.86 / 5.0
• Held weekly office hours to provide conceptual understanding of digital design, computer architecture, and programming assignments
• Helped teach students in class with interactive digital design demonstrations and embedded systems coding

OUTREACH AND VOLUNTEER WORK

ABET External Advisory Board Member, Brown University *Jan 2025*
• Served on the external advisory board with 5 other members for ABET accreditation of the Brown University engineering program

EEMP Curriculum Developer, Science Mentorship Institute *Feb 2024 - Jun 2024*
• Design lecture curriculum to support SCI-MI's 2024 launch of the electrical engineering mentorship program for exposure to research in computer architecture for high school students

ECE Department Representative, UT Austin Graduate Student Assembly *Aug 2023 - Dec 2024*
• Vote on legislation as the graduate student liaison for the Department of Computer and Electrical Engineering at UT Austin
• Relay important information from council meetings to department officials relating to graduate student affairs

Project Manager and Developer, Develop for Good *Sept 2020 - Jan 2021*
• Developed and deployed a Django website for CARE International on analysis and visualization of USAID Hamzari data in an internal website
• Supervised a team of 6 Frontend, Backend, UI/UX developers, and Data Scientists

RELEVANT PROJECTS

Cache Coherence Simulator *Sept 2023 - Dec 2023*
• Designed and implemented a directory-based MESI cache coherence simulator in C++ for up to 32 processors in distributed shared-memory parallel machines

CNN FPGA Hardware Accelerator *Sept 2022 - Dec 2022*
• Designed and deployed CNN accelerator on AWS FPGAs using blocking systolic matrix multipliers on FashionMNIST problem with Xilinx Vitis HLS tools
• Reduced trained parameter sizes by 75% using custom fixed-point 8-bit value representations with little loss to test accuracy.

AWARDS

NSF GRFP Honorable Mention, National Science Foundation *Apr 2024*
Cockrell School of Engineering Fellow, UT Austin *2022-Current*
UT Austin Graduate Excellence Fellow, UT Austin *2022-Current*
Sigma Xi Research Honor Society, Brown University *May 2022*
NSF GRFP Honorable Mention, National Science Foundation *Apr 2022*
Tau Beta Pi Engineering Honor Society, Brown University *Dec 2021*
Grimshaw-Gudewicz Annual Scholar *2020-2022*
Best Use of Google Cloud, Hack @ Brown *Jan 2020*
Valedictorian, Seekonk High School *May 2018*

PROFESSIONAL MEMBERSHIPS

Student Member, IEEE *2021 - Present*
Student Member, ACM *2021 - Present*

SKILLS

Programming Languages
Python, C, C++, Verilog, SystemVerilog, SPICE

Applications

PyTorch, Cadence Virtuoso, Matlab, Gem5, Synopsys HSPICE

Languages
English (Fluent), Cantonese (Fluent)